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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,742	06/20/2003	Chu-Chin Hu	LA-7452-101	5997
167	7590	10/19/2005	EXAMINER	
FULBRIGHT AND JAWORSKI LLP 555 S. FLOWER STREET, 41ST FLOOR LOS ANGELES, CA 90071			NGUYEN, HOA CAO	
			ART UNIT	PAPER NUMBER
			2841	
DATE MAILED: 10/19/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/600,742

Applicant(s)

HU, CHU-CHIN

Examiner

Hoa C. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 9/20/05.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 September 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawing was received on 20 September 2005. The drawing is approved.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1–10 and 12–18 are rejected under 35 U.S.C. 102(e) as being anticipated by Kimura et al. (U.S. Patent 6,806,428 B1).

Regarding claim 1, Kimura et al disclose a library core for embedded passive components comprising:

- a. an insulating core layer 31, see figure 6(a), column 4, lines 18-19; and
- b. a plurality of openings penetrating therethrough 33 and 35, see figures 6(b) and 6(e), column 4, lines 22 and 28; and
- c. a plurality of areas defined by the openings 35 to be filled with passive components 36 and 37, see figure 6(f), column 4, lines 30-32; and
- d. electrically conductive layers 32 and 34 are formed over the upper and lower surfaces of the core layer; see figures 6(a) and 6(e), column 4, lines 19-20 and 25-26.

Regarding claim 2, Kimura et al disclose a plurality of conductive traces 34 for interconnecting between the openings, see figure 6(d), lines 33-38.

Regarding claims 3 and 4, Kimura et al disclose resistors 36 and capacitors 37, see figure 6(f), column 4, lines 30-32.

Regarding claim 5, Kimura et al disclose the conductive traces 34 formed on end electrodes 36a of resistors 36 and therefore partly used as electrodes of the resistors, see figure 6(f), column 4, lines 33-38.

Regarding claim 6, Kimura et al disclose the conductive traces 34 formed on end electrodes 37a of capacitors 37 and therefore partly used as parallel sheets of the capacitors 37, see figure 6(f).

Regarding claim 7, Kimura et al disclose a plurality of conductive vias 33 for interconnecting the conductive layers on the upper and the lower surfaces of the core layer, see figure 6(b), column 4, lines 22-25.

Regarding claim 8, Kimura et al disclose library cores which are inherently a fabrication in a semiconductor packaging substrate or printed circuit board, see figures 1, 7, 8, and 11, the descriptions of the embodiments 1-5, and column 1, lines 46-48.

Regarding claim 9, Kimura et al disclose an insulating layer 5 formed over the conductive traces 4a and so forming a circuit layer on the insulating layer. Conductive vias 9 allows connections between layers and so forming a multi-layer circuit board, see figure 1 and column 2, lines 45-60.

Regarding claims 10, Kimura et al, as shown in figure 1 and column 2, lines 54-58, disclose an IC chip 7 mounted on the multi-layer circuit board and electrically coupled to the conductive traces 4a, 4b, and 4c. The multi-layer circuit board with

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mounted IC chip 7 is inherently a fabrication in a flip-chip semiconductor packaging substrate, because as seen in figure 1, the IC chip 7 is faced down.

Regarding claim 12, Kimura et al disclose a method of forming an electronic device on a library core for embedded passive components comprising the steps of:

- a. Providing an insulating core layer 31 having an upper surface and a lower surface opposed to the upper surface, see figure 6(a), column 4, lines 18-19;
- b. a plurality of openings penetrating therethrough 33 and 35, see figures 6(b) and 6(e), column 4, lines 27-28;
- c. allowing the openings to be filled with passive components 36 and 37, see figure 6(f), column 4, lines 30-32, and
- d. electrically conductive layers 34 and 40 are formed over the upper and lower surfaces of the core layer, see figure 6(a) - 6(i) and column 4, lines 25-44;
- e. patterning the electrically conductive layers respectively on the upper and lower surfaces of the core layer to form a plurality of the conductive traces 34 for electrically interconnecting between the passive components contained in the openings of the core layer, see column 4, lines 33-37; and
- f. mounting and electrically connecting the core with the embedded passive components to the electronic device 7, see figure 1 and column 2, lines 54-58.

Regarding claims 13 and 14, Kimura et al teach the openings 35 are filled with resistors 36 and capacitors 37, see figure 6(f), column 4, lines 30-32.

Regarding claims 15 and 16, Kimura et al teach the conductive traces 34 formed on end electrodes 36a of resistors 36 and therefore partly used as electrodes of

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the resistors, see figure 6(f), column 4, lines 33-38. Kimura et al also teach the conductive traces 34 formed on end electrodes 37a of capacitors 37 and therefore partly used as parallel sheets of the capacitors 37, see figure 6(f).

Regarding claim 17, Kimura et al teach a plurality of conductive vias 33 for interconnecting the conductive layers on the upper and the lower surfaces of the core layer, see figure 6(b), column 4, lines 22-25.

Regarding claims 18, Kimura et al disclose a semiconductor packaging substrate 7 as the electronic device, see figure 1 and column 2, lines 54-58.

Thus, Kimura et al reasonably appear to disclose every limitation of the claims 1-10 and 12-18 therefore anticipates these claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al (U.S. Patent 6,806,428 B1) in view of Okabe et al (U.S. Patent 6,757,178 B2).

Kimura et al, as shown in figures 1 and 6, teach a multi-layer circuit board 1, which is applicable to a flip-chip semiconductor substrate 7, and disclose all the limitations of this claimed invention. However, Kimura et al failed to teach applications to a wire-bonding semiconductor packaging substrate.

Okabe et al, disclose a multi-circuit board for embedded passive components 52 and 53 which is intentionally applicable to a wire-bonding semiconductor packaging substrate 40, see figure 2A, column 4, lines 65 – column 5 line 1.

It would be obvious to one of ordinary skill in this art at the time of invention to have made a wire-bonding semiconductor substrate as taught by Okabe et al on the board of Kimura et al for its simplicity and low potential cost.

Response to Arguments

7. Applicant's arguments filed 9/20/2005 have been fully considered but they are not persuasive.

Regarding the passive components materials and the fully cover both surfaces of the passive component materials (2nd and 4th paragraphs), there is no difference in the structure of the final product with either passive components or passive component materials and there are conductive layers 34 and 40 cover the surfaces with the embedded components.

Regarding the alternating size of the openings (3rd paragraph), Kimura et al. does disclose the alternating size of the openings, see figure 1(a).

Regarding claim 12 (5th paragraph), Kimura et al. disclose every limitation including the order of the steps as shown in claim 12 above.

Regarding the capability of forming the circuit wirings and electrically interconnecting the passive components simultaneously (6th paragraph), this not what in the claim. It is noted that claim 12 does have a step for electrically interconnecting the passive components, the step of "patterning the electrically ...for electrically interconnecting the passive component.....".

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
5 October 2005



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